Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 60 and 61 and amend claims 38, 49-52, and 57-59 as follows:

Listing of Claims:

1-37. (Cancelled)

38. (Currently Amended) An in-process substrate structure including a plurality of contact regions and a plurality of non-contact regions adjacent the contact regions on a surface of the substrate, the in-process substrate structure comprising:

a selectively formed single crystal contact ~~epitaxially grown~~ on each contact region, each single crystal contact being isolated from single crystal contacts on adjacent contact regions, each single crystal contact having ~~a curved~~ an arcuate, convex upper surface intersected by two sidewall surfaces, the two sidewall surfaces being substantially perpendicular to the surface of the substrate.

39-44. (Cancelled)

45. (Previously presented) The substrate of claim 38 wherein the non-contact regions adjacent to the contact region comprise isolation oxide regions.

46. (Previously presented) The substrate of claim 38 wherein the substrate comprises silicon.

47. (Previously presented) The substrate of claim 38 wherein the substrate comprises gallium arsenide.

48. (Previously presented) The substrate of claim 38 wherein the substrate comprises silicon germanium.

49. (Currently Amended) The substrate of claim 38 wherein the single crystal contact comprises silicon.

50. (Currently Amended) The substrate of claim 38 wherein the single crystal contact comprises gallium arsenide.

51. (Currently Amended) The substrate of claim 38 wherein the single crystal contact comprises silicon germanium.

52. (Currently Amended) An in-process semiconductor structure, comprising:

a substrate;

a plurality of active regions;

a plurality of isolation regions adjacent the active regions, each isolation region being positioned between adjacent active regions to isolate adjacent active regions; and

at least one selectively formed single crystal contact ~~epitaxially grown~~ on each active region, each selectively formed single crystal contact being isolated from single crystal contacts on adjacent active regions, each selectively formed single crystal contact having ~~a curved~~ an arcuate, convex upper surface intersected by two sidewall surfaces, the two sidewall surfaces being substantially perpendicular to an upper surface of the active region.

53. (Previously presented) The in-process semiconductor structure of claim 52 wherein each isolation region comprises a field oxide region.

54. (Previously presented) The in-process semiconductor of claim 53 wherein the substrate comprises silicon.

55. (Previously presented) The in-process semiconductor of claim 53 wherein the substrate comprises gallium arsenide.

56. (Previously presented) The in-process semiconductor of claim 53 wherein the substrate comprises silicon germanium.

57. (Currently Amended) The in-process semiconductor of claim 53 wherein each single crystal contact comprises selective epitaxial growth silicon.

58. (Currently Amended) The in-process semiconductor of claim 53 wherein at least some of the single crystal contacts comprise gallium arsenide.

59. (Currently Amended) The in-process semiconductor of claim 53 wherein at least some of the single crystal contacts comprise silicon germanium.

60.-61. (Cancelled)